DEPARTMENT OF INFORMATION TECHNOLOGY				*CLASS: I B.Sc. Information Technology*				
Sem.	**Course Type**	**Course Code**	**Course Title**	**Credits**	**Contact Hours/week**	**CIA**	**Ext**	**Total**
II	Major Core – 4	20U2FMC4	Digital Principles and Applications	2	3	25	75	100

Course Objective:

1. To acquire knowledge on Number systems and Logic gates.
2. To examine the various Logical Expressions.
3. To analyze various Data circuits & Arithmetic operations.
4. To demonstrate the Clocks and Timing Circuits.
5. To characterize various Sequential Circuits.

Unit-I: Number systems and Digital Logic

Binary Number System-Binary to Decimal Conversion-Decimal to Binary conversion -Octal numbers -Hexadecimal numbers -The ASCII code -The Excess-3 code -The Gray Code – transistor inverter. Digital Logic - Basic gates-NOT, OR, AND-Boolean Algebra - Universal logic gates-NOR, NAND.

Unit-II: Combinational logic circuits

Boolean Laws and Theorems -Sum of Products method -Truth table to Karnaugh map -Pairs, Quads, and Octets –Karnaugh simplifications -Don't care condition- Product of sums method -product of sums simplification.

Unit-III: Data Processing circuits

Multiplexers -Demultiplexers -1 of 16 Decoder –BCD to decimal Decoders -Seven segment Decoders. Arithmetic circuits: Binary Addition -Binary Subtraction - 2's & 1's complement Representation -Complement Arithmetic -Arithmetic Building Blocks.

Unit-IV: Flip-Flops and Timers

RS FLIP FLOP- D FLIP- FLOP - JK FLIP-FLOPs – JK MASTER SLAVE FLIP- FLOP. Clocks and Timing circuits: 555 Timer-Astable-555 Timer – Monostable.

Unit-V: Shift Registers and Counters

Types of Registers -Serial-In -Serial-Out-Serial-In -Parallel-Out -Parallel-In-Serial-Out -Parallel-In -Parallel-Out. Counters: Ring Counter – Ripple Counter - Synchronous Counters.

Book for Study

1. Albert Paul Malvino, Donald P.Leach, , Digital Principles and Application, 7thEdn, 2011, McGraw Hill Publication.
   Chapters:
   Unit-I : 1, 4
   Unit-II : 2
   Unit-III : 3.1 to 3.6, 5.1 to 5.7
   Unit-IV : 8.1, 8.3, 8.6, 8.7, 9.3, 9.4
   Unit-V : 10, 11.1, 11.3

Books for Reference

1. Morris Mano, 2005, Digital Logic and computer design, Prentice -Hall of India.
2. RonaldJ.Tocci, 2007, Digital System Principles and Application, Prentice -Hall of India.

Web Resources

1. https://www.tutorialspoint.com/digital_circuits/
2. https://www.electronics-tutorials.ws/sequential/seq_5.html
3. https://soaneemrana.org/onewebmedia/DIGITAL PRINCIPLEs AND Application BY LEACH & MALVINO.pdf

Pedagogy

Chalk and talk , Materials, PPT, Assignment , Seminar , Problem solving , Group discussion , Interaction and Demonstration.

Course Learning Outcomes:

On the successful completion of the course, students will be able to

CLO No.	Course Learning Outcomes	K – Level
CLO1	Illustrate the basic idea about number systems and to learn conversion from one number system to another number system.	Up To K3
CLO2	Examine various logical expressions	Up To K4
CLO3	Analyze various data processing circuits.	Up To K4
CLO4	Explain characteristics of Clocks and Timing Circuits.	Up To K2
CLO5	Compare various sequential circuits.	Up To K2

Mapping of COs with POs:

CLOs/POs	PO1	PO2	PO3	PO4	PO5
CLO1	1	2	1	3	1
CLO2	1	1	1	NA	1
CLO3	1	3	2	NA	2
CLO4	1	3	3	NA	3
CLO5	1	1	3	3	2

3- Advanced Application; 2- Intermediate Level; 1- Basic Level; N/A- Not Applicable

Mapping of CLOs with PSOs:

CLOs / PSOs	PSO1	PSO2	PSO3	PSO4	PSO5	PSO6
CLO1	3	3	3	3	3	3
CLO2	3	3	3	3	3	3
CLO3	3	2	3	2	3	2
CLO4	2	2	2	1	2	1
CLO5	2	1	2	1	3	1

3- Advanced Application; 2- Intermediate Level; 1- Basic Level; N/A- Not Applicable

Learning Outcome Based Education & Assessment (LOBE)
Blue Print for Summative Examination - Digital Principles and Applications
Articulation Mapping – K Levels with Course Learning Outcomes (CLOs)

Sl.No	CLOs	K - Level	Section A		Section B		Section C (Either / or Choice)	Section D (Open Choice)
			MCQs		Short Answer			
			No. of Questions	K – Level	No. of Questions	K - Level		
1	CLO 1	Up to K 3	2	K3 & K3	1	K3	2 (K3 & K3)	1(K3)
2	CLO 2	Up to K 4	2	K4 & K4	1	K4	2 (K3 & K3)	1(K4)
3	CLO 3	Up to K 4	2	K1 & K2	1	K2	2 (K2& K2)	1(K4)
4	CLO 4	Up to K 3	2	K1 & K2	1	K3	2 (K3 & K3)	1(K2)
5	CLO 5	Up to K 2	2	K1 & K2	1	K1	2 (K1 & K1)	1(K2)
No. of Questions to be asked			10		5		10	5
No. of Questions to be answered			10		5		5	3
Marks for each Question			1		2		5	10
Total Marks for each section			10		10		25	30

K1 – Remembering and recalling facts with specific answers
K2 – Basic understanding of facts and stating main ideas with general answers
K3 – Application oriented – Solving Problems
K4 – Examining analyzing , presentation and make inferences with evidences

Distribution of Section – wise Marks with K Levels

K – Level	Section A (No Choice)	Section B (No Choice)	Section C (Either / or Choice)	Section D (Open Choice)	Total Marks	% of Marks without choice	Consolidated
K1	3	2	10	-	15	12.5	42%
K2	3	2	10	20	35	29.16	
K3	2	4	30	10	46	38.33	38%
K4	2	2	-	20	24	20	20%
Total Marks	10	10	50	50	120	100.00	100 %

Lesson Plan:

Units	Topic	Hours	Mode
I	Binary Number System-Binary to Decimal conversion-Decimal to Binary conversion -Octal numbers -Hexadecimal numbers -The ASCII code -The Excess-3 code -The Gray Code.	6	Lecture, GD
	Basic gates-NOT, OR, AND-Boolean Algebra - Universal logic gates-NOR, NAND.	3	Lecture
II	Combinational logic circuits Boolean Laws and Theorems -Sum of Products method -Truth table to Karnaughmap -Pairs, Quads, and Octets – Karnaugh simplifications -Don't care condition.	6	Lecture, GD
	Product of sums method -product of sums simplification.	3	Lecture, GD
III	Multiplexers -Demultiplexers -1 of 16 Decoder –BCD to decimal Decoders -Seven Segment Decoders.	6	Lecture
	Binary Addition -Binary Subtraction - 2's & 1's complement Representation -Complement Arithmetic -Arithmetic Building Blocks.	3	Lecture& GD
IV	RS FLIP FLOP- D FLIP- FLOP - JK FLIP-FLOPs – JK MASTER SLAVE FLIP- FLOP.	5	Lecture
	555 Timer-Astable - Monostable.	4	Lecture
V	Types of Registers -Serial-In -Serial-Out-Serial-In -Parallel-Out -Parallel-In-Serial-Out -Parallel-In -Parallel-Out.	5	Lecture, PPT
	Ring Counter – Ripple Counter - Synchronous Counters.	4	Lecture, Assignment

Name of the Course Designers:

1. Mrs. S. Sasikala
2. Mrs. S. Rajalakshmi